MEMS High Q Microwave Inductors Using Solder Surface Tension Self-Assembly

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***Abstract* — We present microwave inductors of 1.5 to 2.5 nH fabricated out-of-plane by a self-assembly process. The consequent de-coupling from the substrate allows improved Q (from 4 to 20) and frequency of maximum Q (from 0.5 GHz to 3 GHz) on low resistivity silicon substrates.**

I. Introduction

Availability of good quality microwave inductors is a major restraint in achieving higher levels of integration in monolithic microwave ICs. Conventional planar on-chip inductors suffer from parasitic capacitance and losses due to capacitive and inductive coupling into the substrate, which results in low self-resonant frequency and low Q factor.

A new solution to these limitations has arisen with recent progress in MEMS (microelectromechanical systems) fabrication technologies, which allows the realisation of increasingly complex structures. In the case of microwave inductors, much research effort has been applied to separating the current carrying coil from the lossy substrate, an obvious approach to reducing the parasitics.

Recent publications include fabrication of inductors on thick dielectrics [1], airbridged inductors [2] and various techniques based on removal of the substrate underneath the coil [3]-[5]. A serious problem with these approaches is the limited separation that can be achieved (only tens of μm or less). Moreover, for techniques involving substrate etching there are concerns about process compatibility, and the reduced mechanical stability of the substrate.

Another approach which is similar to the one presented herein uses scratch drive actuators [6] to buckle up the inductor mounted on a Si support structure. This has the disadvantage of chip area being lost for the assembly mechanism. Finally a recent publication introducing a process for the fabrication of solenoid coils [7] has the drawback of involving non-parallel processing, i.e. direct writing lithography.

Our approach, in contrast, is based on a fully parallel batch process and, at the same time, allows a very substantial separation between coil and substrate (several hundreds of μm). Moreover, further reduction of capacitance and inductive substrate coupling is achieved by rotating the coil into a plane perpendicular to the substrate.

II. Fabrication

The self-assembly technique presented here follows previous developments by this group [8]-[10]. Using a planar process, copper structures are fabricated with solder pads being placed between an anchored and a released portion of the devices. When the wafer is heated, the solder pads are melted, acting as hinge drives through the surface tension force that occurs, and rotating the structures out of the substrate plane. The wafer is then cooled down, the solder pads resolidify and the structure remains assembled. Inductors that have been fabricated and a close-up on the hinge region before and after self-assembly are shown in figures 1 and 2.

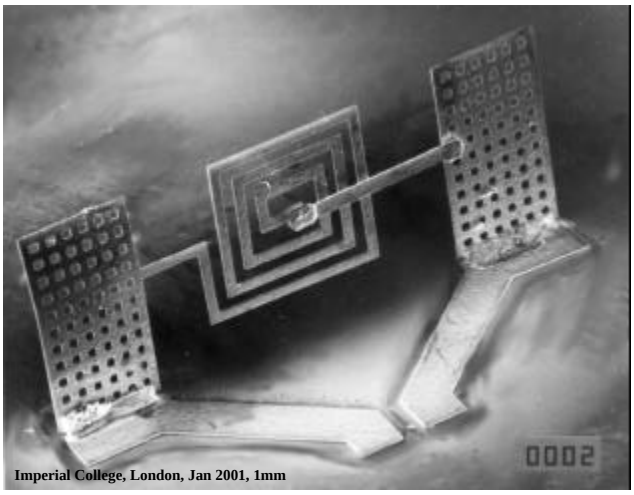

Fig. 1. 3-turn spiral inductors after self-assembly

The planar fabrication of the devices is carried out in a five layer surface micromachining process (three layers for meander inductors), involving only UV lithography, and copper and lead/tin solder electroplating as deposition

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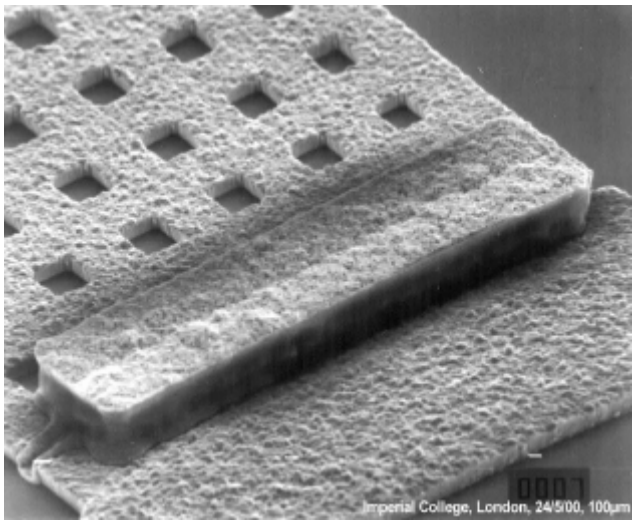
techniques. Conventional positive photoresist is used as a sacrificial layer, thus any harsh etching technique or substrate removal is avoided. Moreover, the peak process temperature is low, a maximum of 183°C being required to reflow the solder pads. As a result, the process is compatible with any common substrate type, and also with CMOS or typical MMIC pre-processed structures.



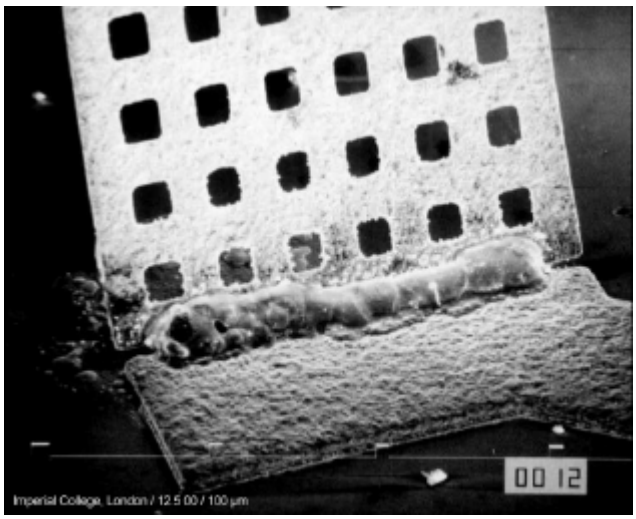


Fig. 2. Solder hinges before (top) and after (bottom) self-assembly.

Two different types of inductors have been fabricated: spiral (figure 1) and meander inductors (figure 3). Quite obviously, the meander coil geometry has the drawback of yielding less inductance for the same chip area and having lower Q due to increased track length, but on the other hand the fabrication process is less complex, since no airbridge is required and hence two process layers can be avoided.

In the first instance, meander inductors have been realised and these have been characterised up to 5GHz. The results are presented in the following paragraph. The fabrication of spiral inductors has only been achieved very recently and reliable measurements are not available yet.

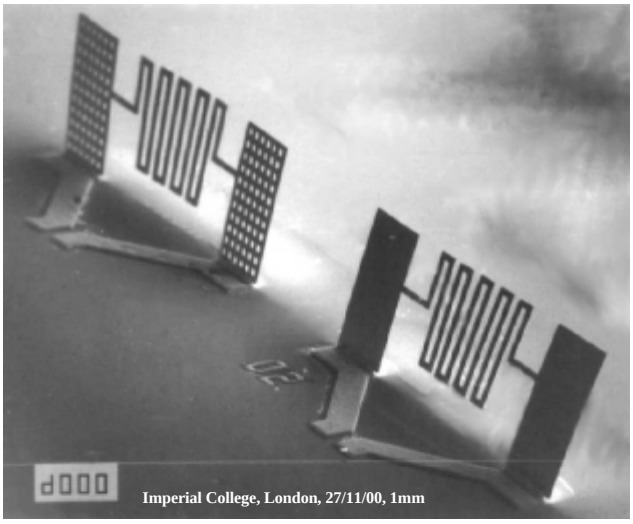


Fig. 3. 4½-turn meander inductors after self-assembly

III. Results

Measurements were obtained using the single-sweep HP 8510XF network analyser, having 1 mm coaxial cables, and Cascade Microtech probes. Calibration was performed using Cascade Microtech's alumina LRRM impedance standard substrate (ISS) and WinCal software. A dielectric chuck was placed under the ISS to ensure that the correct modes were excited.

The conductivity of the Si substrate was extracted from the measurements by comparison with Sonnet EM models of the planar inductor structures. This value was then used to model the feed lines and deembed them from the measured results. The following definition for the quality factor was used:

$$Q = \frac{\mathrm{Im}\{Z\}}{\mathrm{Re}\{Z\}} \qquad (1)$$

Table 1 gives measured device characteristics for different coil geometries. All devices have the same overall dimensions of approximately 1.2 mm x 0.5 mm, and coil dimensions of 0.35 mm x 0.35 mm. In order to realise different inductance values, only the track width and the spacing between the track is varied, while outer dimensions are kept constant.

type	L [nH]	peak Q	f_{peak} [GHz]
3-turn meander	1.5	17	3.5
4½-turn meander	2.0	20	3
6-turn meander	2.5	13	3
2-turn spiral	2.0	n/a	n/a
3-turn spiral	3.5	n/a	n/a
4-turn spiral	5.5	n/a	n/a

Tab 1. Measured device characteristics for different coil geometries, after self-assembly (upright)

Figure 4 and 5 illustrate the effect of the separation of the coil from the substrate through our self-assembly technique. The figures show quality factor and real part of the impedance, respectively, for different folding angles between the coil and the substrate.

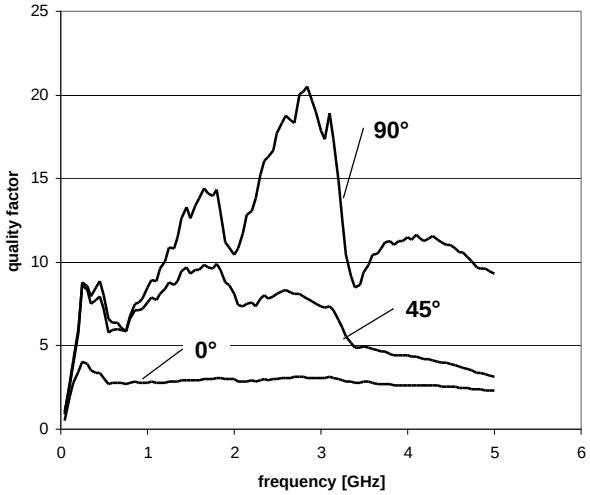


Fig. 4. Quality factor versus frequency for different angles between coil and substrate, all devices 4½-turn meander inductors (L ≅ 2 nH)

As expected there is a very significant increase in peak Q and in f_{max} (frequency at which peak Q is reached) which is due to the reduction in coil to substrate capacitance and the reduction in substrate coupling. A device that is not folded (but released from the substrate, separated by a 3 µm air gap) only reaches a Q of 4 at around 0.5 GHz. In contrast, a device standing upright on the substrate achieves a Q of 21 at 3GHz. The effective separation from the substrate is 300 µm at the centre of the coil. Fig. 5 highlights the increase of the losses for different folding angles. With all devices having the same DC resistance, a very drastic reduction in substrate losses for the folded devices can be observed.

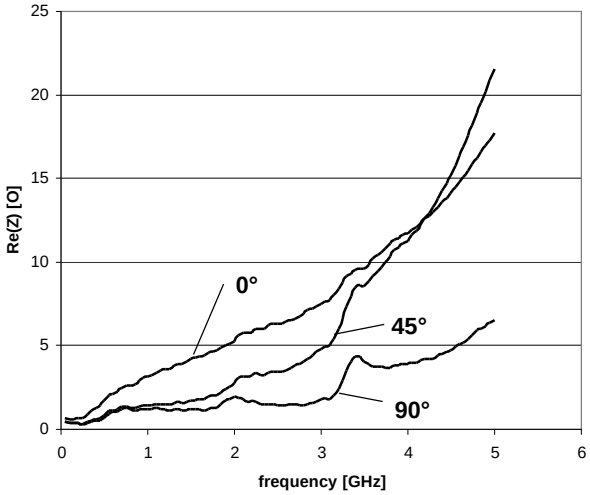


Fig. 5. Real part of impedance versus frequency for different angles between coil and substrate; all devices are 4½-turn meanders (L ≅ 2 nH).

IV. Conclusion

Rotation of copper meander inductors into a vertical plane has been shown to provide substantial increases in quality factor, and in frequency of maximum Q. Values of Q up to 20 have been achieved, at 3 GHz, for 2 nH inductors on low resistivity silicon. The fabrication process is fully parallel, involves no high temperatures, substrate removal or electrochemical etching, and is expected to be compatible with post-processing on CMOS or MMIC wafers.

Acknowledgements

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